Clustered Timing Model: Statistical Modeling of Variability for Dynamic Estimation of Errors

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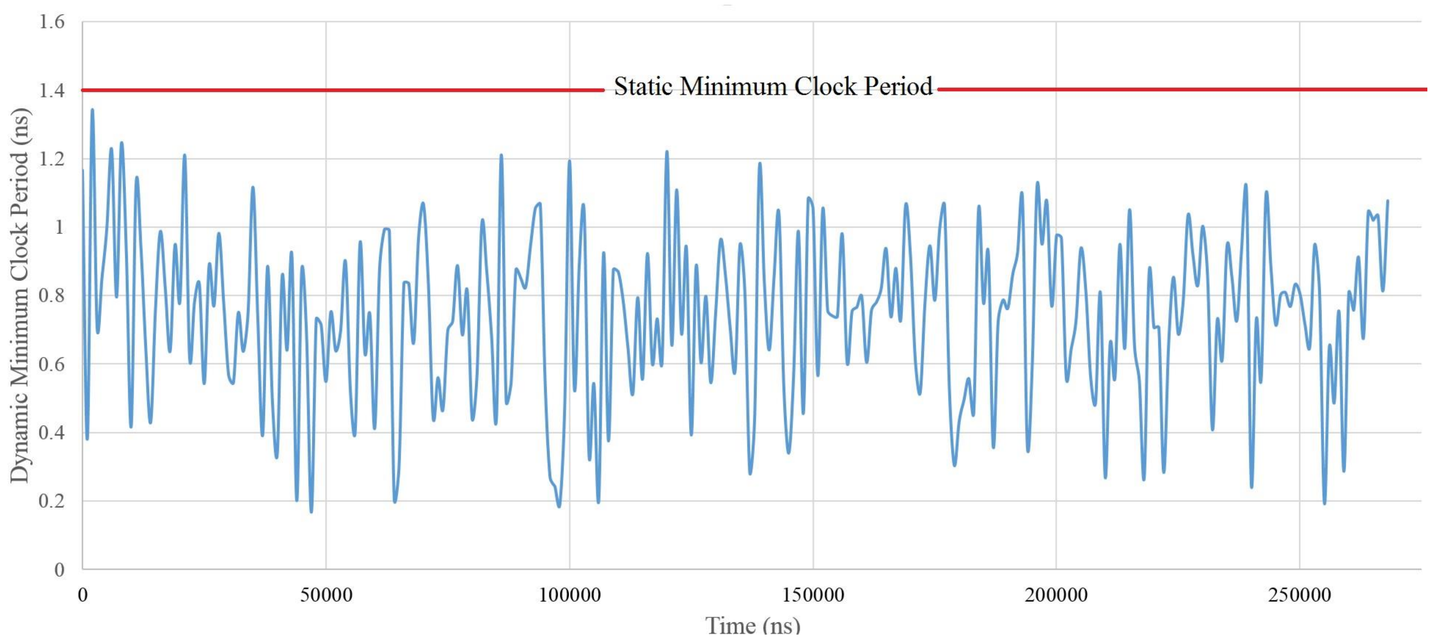
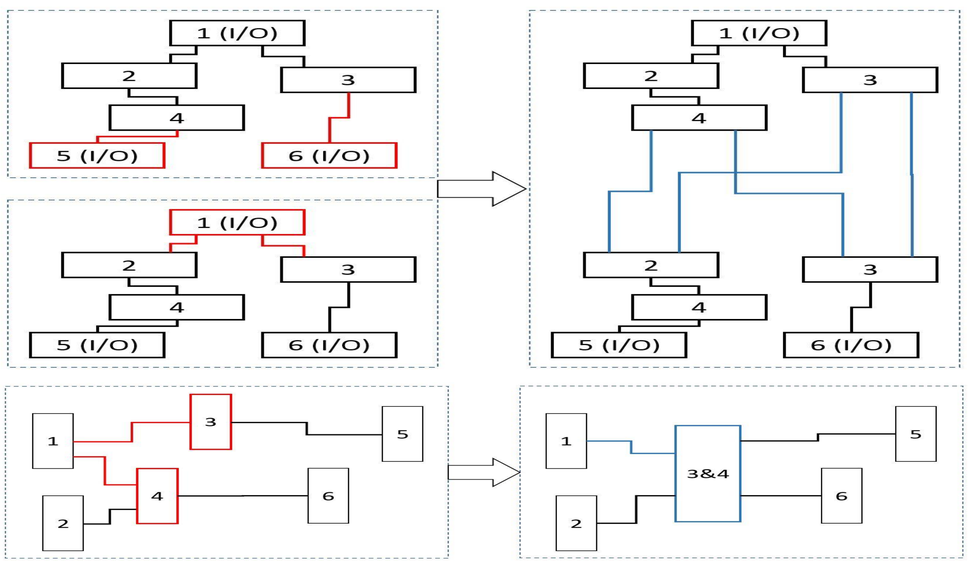
Motivation

The behavior of CMOS circuits is increasingly susceptible to variations in the manufacturing process and environmental conditions. The traditional hardware-to-software model consisting of a set of instructions with fixed and deterministic timing and functional behaviors is no longer sufficient. The new models need to dynamically predict the next state of the system based on the software it is running and the environmental conditions it is placed in, and be aware of the non-determinism due the physical variations.





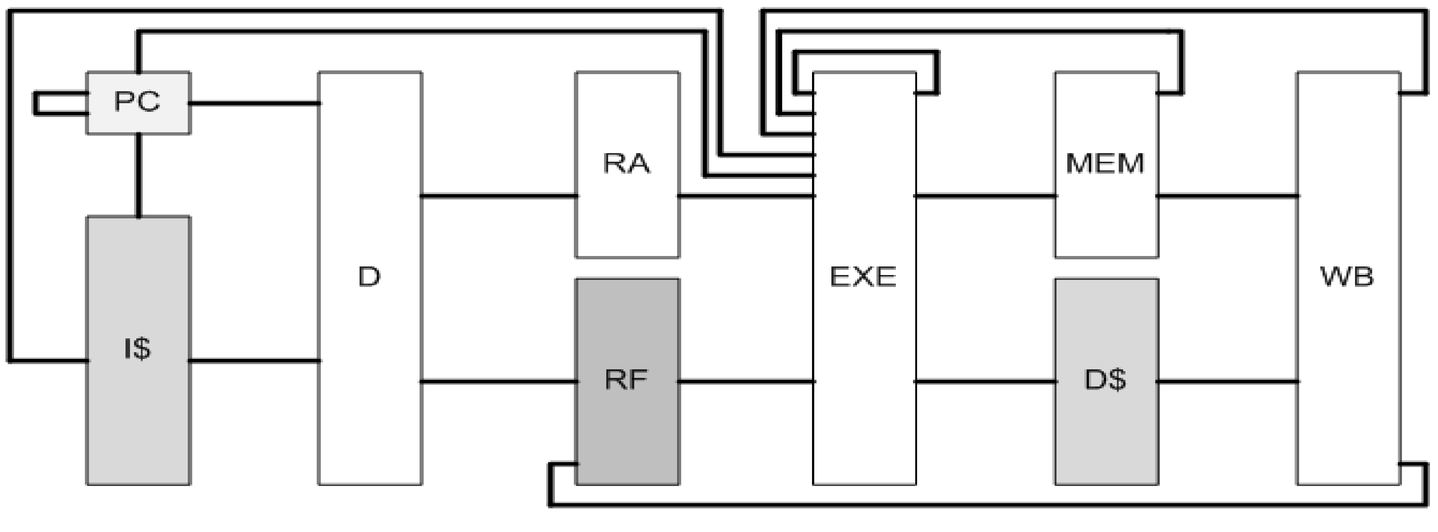
Clustered Timing Model

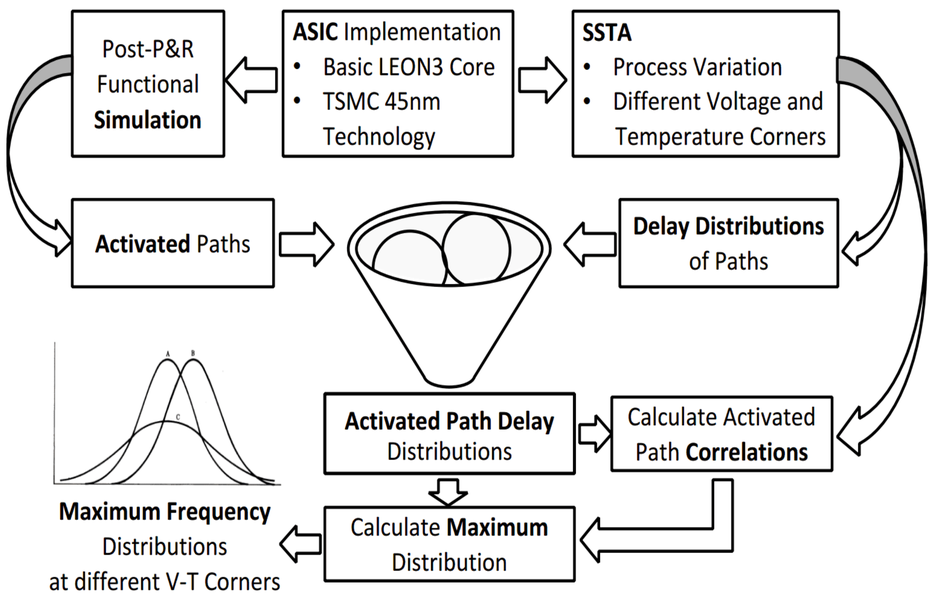
The *State* of a sequential circuit consists of the contents of all its registers (including memory cells) and its primary I/O which together we call *state storing elements*. *State Storing Element Clustering* defines an equivalence relation on the state of the circuit, partitioning its state storing elements into a set of ***State Storing Clusters* (SSCs)** and the paths into ***hyperpaths***. There is a hyperpath between two SSCs when there is at least one timing path connecting a state storing element output in the *origin* SSC to a state storing element input in the *destination* SSC. Therefore, there can be zero, one, or two hyperpaths between two SSCs. The resulting model is called a ***Clustered Timing Model (CTM)***.

A CTM for LEON3

One state storing clustering for LEON3 assigns an SSC to each pipeline stage register, an SSC to the PC, an SSC to the register file, and two SSCs to the caches, dividing the hyperpaths into four types:

I. ***Data Transfer hyperpaths***
II. ***Addition hyperpaths***
III. ***Logic hyperpaths***
IV. ***Hybrid hyperpaths***





Processor Characterization and Results

		Hyperpaths																		
	Org	PC	PC	PC	I$	D	D	RA	RF	EXE	EXE	EXE	EXE	EXE	MEM	MEM	D$	WB	WB	Avg
	Dst	PC	I$	D	D	RA	RF	EXE	EXE	I$	PC	EXE	MEM	D$	EXE	WB	WB	EXE	RF	
(V,T)	(0.99,-40)	4.3	2.2	2.3	1.7	5.2	5.8	3.9	2.6	4.1	4.3	4.6	4.7	4.5	4.8	3.1	2.9	4.9	2.1	3.8
	(0.81,125)	5.2	2.0	2.7	1.9	5.5	5.0	3.8	2.5	4.9	4.3	4.8	6.4	4.4	4.2	3.5	2.6	6.1	2.1	4.0
	(0.99,0)	4.5	2.1	2.5	1.8	5.8	5.2	3.5	2.8	4.7	3.9	4.5	5.6	4.0	4.5	3.4	2.8	6.7	2.0	3.9
	(0.81,0)	4.3	2.1	2.2	1.7	5.5	5.9	3.8	2.4	4.2	4.9	4.3	4.5	4.3	4.5	3.1	3.1	4.5	2.3	3.8
	(0.81,-40)	4.3	2.3	2.4	1.9	6.0	5.7	3.4	2.4	4.8	4.2	5.5	4.3	4.9	4.9	3.4	3.2	6.4	2.2	4.0
	Avg	4.5	2.1	2.4	1.8	5.6	5.5	3.7	2.5	4.5	4.3	4.7	5.1	4.4	4.6	3.3	2.9	5.7	2.1	3.9

NSF Expedition in Computing, Variability-Aware Software for Efficient Computing with Nanoscale Devices http://variability.org

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