Omid Assare

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Background

Background in broad areas of **digital design**, **electronic design automation**, and **computer architecture**.
Extensive experience in **C++ software development** for performance analysis at various levels of the hardware-software stack.
Proficient in **hardware development in Verilog** and other hardware description languages as well as ASIC and FPGA design tools.

Education

June 2019 — Department of Computer Science and Engineering | University of California San Diego
- **PhD in Computer Engineering,** Performance Analysis of Timing-Speculative Processors
- **MS in Computer Engineering,** Error Detection and Correction Techniques for Timing-Speculative Processors
- **Advisor :** Rajesh Gupta

September 2012 — Electrical Engineering Department | Sharif University of Technology
- **BS in Electrical Engineering,** Modeling Power Consumption of VLSI Circuits under Process Variation

Skills

Programming Languages	C, C++, Java, Python
Hardware Description Languages	Verilog, VHDL, SystemVerilog, Bluespec SystemVerilog (BSV)
Assembly Languages	SPARC, ARM, MIPS, x86, OpenRISC
ASIC Design Tools	Synopsys Design Compiler, Synopsys IC Compiler, Synopsys PrimeTime
FPGA Design Tools	Xilinx ISE, Intel/Altera Quartus
Logic Simulation Tools	Modelsim, HSPICE
Statistical Analysis	MATLAB, R
Compiler/Code Analysis	LLVM, Intel Pin

Professional Experience

June 2019 – September 2012 — Research Assistant | Microelectronic Embedded Systems Laboratory

- **Statistical Dynamic Timing Analysis.** Developed a timing analysis engine based on path activation analysis that makes characterization of design-time uncertainty such as process variation possible.
  Design Compiler | IC Compiler | PrimeTime | Python | Modelsim

- **Cross-Layer Timing Error Prediction.** Developed a high-level model that predicts if a specific combination of physical parameters in hardware and data variations in software will produce a timing error more than 20,000 times faster than widely-used gate-level analysis while losing no more than 6.4 percent in accuracy.
  C++ | VHDL | SPARC

- **Application-Specific Performance Analysis of Timing-Speculative Processors.** Developed a statistical performance analysis framework that enables design and evaluation of aggressive frequency and voltage scaling schemes by quantifying an application's vulnerability to timing errors and its sensitivity to variations in program input data and physical parameters of the processor.
  MATLAB | LLVM | C++

- **Timing Speculation Strategies.** Developed a software-directed dynamic frequency scaling scheme that improved throughput of a timing-speculative processor by more than 50 percent compared to the conventional design while incurring little power overhead.
  LLVM | C | C++ | SPARC

September 2012 – September 2010 | Research Assistant | Energy-Aware Systems Laboratory

- **Modeling Standard Cell Leakage Current.** Developed a variation-aware leakage current model for a standard cell library that closely tracks HSPICE simulation data by examining all major considerations at the transistor level, including major sources (threshold voltage and effective channel length) and types (intra-die and inter-die) of process variation as well as other complicating issues such as DIBL effect.
  Design Compiler | HSPICE | MATLAB

- **Full-Chip Leakage Power Estimation.** Proposed a Monte Carlo based, highly accurate framework for estimation of full-chip leakage power distribution in presence of process variation.
  Verilog | OpenRISC | R | MATLAB

- **System-Level Power Reduction Techniques.** Analyzed benefits of software-based techniques to improve power consumption of an OpenRISC embedded processor core implemented on FPGA.
  C | OpenRISC | Quartus | Modelsim

Publications

Accurate Estimation of Program Error Rate for Timing-Speculative Processors
Omid Assare and Rajesh Gupta
*The 56th IEEE/ACM Design Automation Conference (*DAC*), June 2019*

Strategies for Optimal Operating Point Selection in Timing-Speculative Processors
Omid Assare and Rajesh Gupta
*The 32nd IEEE International Conference on Computer Design (*ICCD*), October 2016*

Yield-Driven Design-Time Task Scheduling Techniques for MPSoCs under Process Variation : A Comparative Study
Mahmoud Momtazpour, **Omid Assare**, Negar Rahmati, Amirali Boroumand, Saeed Barati, and Maziar Goudarzi
IET Journal of Computers and Digital Techniques, Volume 9, Issue 4, July 2015

Timing Analysis of Erroneous Systems
Omid Assare and Rajesh Gupta
*International Conference on Hardware/Software Co-Design and System Synthesis (*CODES+ISSS*), October 2014*

Clustered Timing Model : Statistical Modeling of Variability for Dynamic Estimation of Errors
Omid Assare and Rajesh Gupta
*The 51st IEEE/ACM Design Automation Conference (*DAC*), June 2014 (poster)*

Leak-Gauge : A Late-Mode Variability-Aware Leakage Power Estimation Framework
Omid Assare, Mahmoud Momtazpour, and Maziar Goudarzi
*Elsevier Journal of Microprocessors and Microsystems (*MICPRO*), Volume 37, Issue 8, Part A, November 2013*

Accurate Estimation of Leakage Power Variability in Sub-Micrometer CMOS Circuits
Omid Assare, Mahmoud Momtazpour, and Maziar Goudarzi
*The 15th Euromicro Conference on Digital System Design (*DSD*), September 2012*
Nominated for Best Paper Award

Opportunities for Embedded Software Power Reductions
Omid Assare and Maziar Goudarzi
*The 24th IEEE Canadian Conference on Electrical and Computer Engineering (*CCECE*), May 2011*